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EXAMINER	
PERILLA, JASON M	
ART UNIT	**PAPER NUMBER**
2638	

DATE MAILED: 12/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/043,700	RHODES ET AL.	
	Examiner	Art Unit	
	Jason M. Perilla	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-16 and 18-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-16 and 18-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9, 11-16, and 18-22 are pending in the instant application.

Claim Objections

2. Claim 15 is objected to because of the following informalities:

Regarding claim 14, in line 3, "a first signal port" should be replaced by –the first signal port".

Regarding claim 15, in line 8, "the respective capacitor" is indefinite because the claim provides for "a respective capacitor" in line 4 and "by respective capacitors" in line 6. Therefore, it is not possible to determine which capacitor is referred to by "the respective capacitor" of line 8.

Regarding claims 21 and 22, each instance of "pin diode" should be replaced by "PIN diode" for claim consistency in the application.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 7, 11, 14, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atokawa (US 6308051 – previously cited) in view of Shimo (US 5193218) and in further view of Osofsky et al (US 6724840; hereafter "Osofsky").

Regarding claim 1, Atokawa discloses a multi-mode bidirectional communications device, comprising: a diplexer (fig. 1) having a high-pass filter (fig. 1, ref. 27), a low-pass filter (fig. 1, ref. 28), a digital control input (fig. 1, ref. CONT2) connected in signal communication with he low-pass filter, and a notch filter (fig. 1, refs. D3, L4, R2, and C13) selectively coupled to the low-pass filter by the digitally operable switch in response to indicium of a desired spectral region (col. 5, lines 47-61). The purpose of the diplexer of Atokawa is to couple both a high frequency signal and a low frequency signal upon a single channel. In the case of Atokawa, the channel is accessed by the antenna (fig. 1, "ANT"). Atokawa discloses that the design of the diplexer is such that the transmitting circuit or high pass filter (fig. 1, ref. 27) is a high impedance to low frequency signals while the receiving circuit or low pass filter (fig. 1, ref. 28) is a high impedance to high frequency signals (col. 1, lines 30-35). Further, the low pass filter of Atokawa has a selectable "notch" filter (fig. 1, refs. D3, L4, R2, and C13) that may be selectively coupled to the low pass filter by a control voltage (fig. 1, ref. "CONT2") in response to a desired spectral response of the filter. The control pin CONT2 is asserted in either an "ON" or "OFF" position (col. 8, lines 4-11). Therefore, the control pin takes a digital (on/off) input. Atokawa does not disclose that the communications device asserts the control voltage using a digitally operable switch responsive to signals from a microprocessor. However, Shimo teaches the use of digitally operable transistor switches (fig. 5, refs. 71 and 72) in signal communication with a control circuit (fig. 5, ref. 6) to modify a filter response (col. 2, lines 39-68). As understood by one having skill in the art, the transistor switches provide a digital

interface to an analog circuit. That is, the switches allow for the analog filter to be controlled by a digital control circuit (fig. 5, ref. 6; col. 4, lines 29-35). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a transistor switch and control circuit as taught by Shimo to assert the control pin of the communication device of Atokawa because it would allow for a low power digital control voltage from a control circuit to be interfaced with the analog portions of the communication device.

Further regarding claim 1, Atokawa in view of Shimo disclose a communication device with a digitally operable switch coupled to a control circuit, but do not explicitly disclose that the control circuit is a *microprocessor*. However, Osofsky teaches a microprocessor (fig. 1B, ref. 50) control circuit which digitally controls a tunable communications device (fig. 2) using digital control input pins (fig. 2, refs. D4, D3). As notoriously known by those having skill in the art, microcontrollers are advantageous controllers because they can be programmed to perform a multiplicity or various functions. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a microprocessor as taught by Osofsky as the control circuit in the communications device of Atokawa in view of Shimo because it is an effective and adaptable digital controller.

Regarding claim 7, Atokawa in view of Shimo, and in further view of Osofsky disclose the limitations of claim 1 as applied above. Further, Atokawa discloses that the high pass filter passes signals greater than 88Mhz (col. 1, lines 30-35). That is, the high pass filter passes the transmission frequency signals of 887-925Mhz.

Regarding claim 11, Atokawa in view of Shimo, and in further view of Osofsky disclose the limitations of claim 10 as applied above. Further, Shimo discloses that the digitally operable switch is a transistor (fig. 5, ref. 71)

Regarding claim 14, Atokawa in view of Shimo, and in further view of Osofsky disclose the limitations of claim 14 as applied to claim 1 above.

Regarding claim 18, Atokawa in view of Shimo, and in further view of Osofsky disclose the limitations of claim 14 as applied above. Further, Shimo discloses that the selector switch is a transistor (fig. 5, ref. 71).

5. Claims 14, 15, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atokawa (US 6414566; hereafter "Atokawa-'566" – previously cited) in view of Osofsky.

Regarding claim 14, Atokawa-'566 discloses a multi-mode bidirectional communications device (abstract; fig. 1), comprising: a diplexer (fig. 1, "DUPLEXER"; fig. 2) having a high-pass filter between a first signal port and a second signal port (fig. 2, between ANT and RX terminals), a low-pass filter between the first signal port and a third signal port (fig. 2, between ANT and TX terminals), a digitally operable switch (fig. 2, refs. D1 and D2) connected in signal communication with said low-pass filter, and a notch filter (fig. 2, refs. C20, C10, LT2, LT1) selectively (fig. 2, refs. D1, D2, CONT1) coupled to the low-pass filter by the digitally operable switch in response to indicium of a desired spectral region (col. 2, lines 30-45; col. 5, lines 35-50). Atokawa-'566 discloses a communication device with a digitally operable switch but does not explicitly disclose that the switch is responsive to signals from a *microprocessor*. However, Osofsky

teaches a microprocessor (fig. 1B, ref. 50) control circuit which digitally controls a tunable communications device (fig. 2) using digital control input pins (fig. 2, refs. D4, D3). As notoriously known by those having skill in the art, microcontrollers are advantageous controllers because they can be programmed to perform a multiplicity or various functions. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a microprocessor as taught by Osofsky as an input to the digital switch of Atokawa-'566 because it is an effective and adaptable digital controller.

Regarding claim 15, Atokawa-'566 in view of Osofsky disclose the limitations of claim 14 as applied above. Further, Atokawa-'566 discloses a first plurality of inductors (fig. 2, refs. L2, L1, and L31) connected in series between said first (fig. 2, ANT) and third signal ports (fig. 2, ref. TX), each of said first plurality of inductors being coupled to ground via a respective capacitor (fig. 2, refs. C21, C11) forming thereby a plurality of single pole filter elements, a portion of said first plurality of inductors being bypassed by respective capacitors (fig. 2, refs. C20, C10), the portion consisting of any of the first plurality of inductors which are connected to said notch filter (fig. 2, refs. C20, C10, LT2, LT1, D2 and D1) via the respective capacitor; and said notch filter comprises: a second plurality of inductors (fig. 2, refs. LT1, LT2), where each inductor is respectively coupled between a portion of the capacitors of the single pole filter elements of the low-pass filter and ground (fig. 2).

Regarding claim 19, Atokawa-'566 in view of Osofsky disclose the limitations of claim 15 as applied above. Further, Atokawa-'566 discloses that the digitally operable

switch comprises a plurality of PIN diodes (fig. 2, refs. D2 and D1; col. 5, lines 50-55) respectively coupled in parallel with said second plurality of inductors (fig. 2, refs. LT1, LT2), wherein said PIN diodes are adapted for connection to a control signal (CONT1) from the microprocessor (Osofsky; fig. 1B, ref. 50) for selectively biasing the PIN diodes to couple and decouple the notch filter to the low-pass filter.

6. Claims 1, 2, 8, 14, 15, 16, and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atokawa-'566 in view of Shimo and in further view of Osofsky.

Regarding claim 1, Atokawa-'566 discloses a multi-mode bidirectional communications device (abstract; fig. 1), comprising: a diplexer (fig. 1, "DUPLEXER"; fig. 2) having a high-pass filter (fig. 2, between ANT and RX terminals), a low-pass filter (fig. 2, between ANT and TX terminals), and a notch filter (fig. 2, refs. C20, C10, LT2, LT1) selectively coupled (fig. 2, refs. CONT1) to the low-pass filter in response to indicium of a desired spectral region (col. 2, lines 30-45; col. 5, lines 35-50). Further, Shimo and Osofsky teach the digitally operable switch connected in signal communication with the low-pass filter and responsive to signals from a microprocessor as applied in the rejection of claim 1 as being unpatentable over Atokawa in view of Shimo, and in further view of Osofsky, above.

Regarding claim 2, Atokawa-'566 in view of Shimo, and in further view of Osofsky disclose the limitations of claim 1 as applied above. Further, Atokawa-'566 discloses upstream processing circuitry (fig. 1, "TRANSMITTER CIRCUIT") and downstream processing circuitry (fig. 1, "RECEIVER CIRCUIT") coupled to said diplexer.

Regarding claim 8, Atokawa-'566 in view of Shimo, and in further view of Osofsky disclose the limitations of claim 2 as applied above. Further, Atokawa-'566 discloses that said upstream processing circuitry (fig. 1, "TRANSMITTER CIRCUIT") is selectively coupled to one of said low-pass filter and said low-pass filter in conjunction with said notch filter (fig. 1, "TRANSMITTING FILTER"; fig. 2, filter between "ANT" and "TX").

Regarding claim 14, Atokawa-'566 in view of Shimo, and in further view of Osofsky disclose the limitations of claim 14 as applied to claim 1 above.

Regarding claim 15, Atokawa-'566 in view of Shimo, and in further view of Osofsky disclose the limitations of claim 14 as applied above. Further, Atokawa-'566 discloses a first plurality of inductors (fig. 2, refs. L2, L1, and L31) connected in series between said first (fig. 2, ANT) and third signal ports (fig. 2, ref. TX), each of said first plurality of inductors being coupled to ground via a respective capacitor (fig. 2, refs. C21, C11) forming thereby a plurality of single pole filter elements, a portion of said first plurality of inductors being bypassed by respective capacitors (fig. 2, refs. C20, C10), the portion consisting of any of the first plurality of inductors which are connected to said notch filter (fig. 2, refs. C20, C10, LT2, LT1, D2 and D1) via the respective capacitor; and said notch filter comprises: a second plurality of inductors (fig. 2, refs. LT1, LT2), where each inductor is respectively coupled between a portion of the capacitors of the single pole filter elements of the low-pass filter and ground (fig. 2).

Regarding claim 16, Atokawa-'566 in view of Shimo, and in further view of Osofsky disclose the limitations of claim 14 as applied above. Further, Atokawa-'566 discloses that said high-pass filter (fig. 2) comprises: a plurality of capacitors (fig. 2, refs.

C34, C45) connected in series between said first (RX) and second signal ports (ANT), each of said capacitors being coupled to ground via serially coupled circuit elements (fig. 2, refs. L3 & C30, L5 & C50) forming thereby a plurality of single pole filter elements, each of said serially coupled circuit elements comprising a capacitor and inductor.

Regarding claim 20, Atokawa-'566 discloses a method of passing bi-directional communications signals of differing modes through a diplexer (fig. 1; abstract) having a high-pass filter coupled between a first (fig. 2, "ANT"; fig. 1, "ANTENNA PORT") and a second signal port (fig. 2, "TX"; fig. 1, "TRANSMITTED-SIGNAL INPUT PORT), a first low-pass filter selectively coupled to a notch filter (fig. 2, refs. C20, C10, LT2, LT1, CT, and RT), said low-pass filter coupled between the first and a third signal port (fig. 2, "RX"; fig. 1, "RECEPTION SIGNAL OUTPUT PORT), comprising: receiving downstream signals at the first signal port; filtering the received downstream signals using said high-pass filter (fig. 1, "RECEIVING FILTER); communicating filtered downstream signals to the second signal port (fig. 1, "RECEPTION SIGNAL OUTPUT PORT); receiving upstream signals at the third signal port (fig. 1, "TRANSMITTED-SIGNAL INPUT PORT); selectively coupling said notch filter to the low-pass filter (fig. 2, between ANT and TX terminals) for filtering the received upstream signals in response to a desired communications mode (col. 5, lines 35-50); and sending the filtered signals to the first signal port (fig. 1, "ANTENNA PORT"). Further, Shimo and Osofsky teach the digitally operable switch connected in signal communication with the low-pass filter and responsive to signals from a microprocessor as applied in the rejection of claim 1 as

being unpatentable over Atokawa in view of Shimo, and in further view of Osofsky, above.

Regarding claim 21, Atokawa-'566 in view of Shimo, and in further view of Osofsky disclose the limitations of claim 1 as applied above. Further, Atokawa discloses that the notch filter comprises a plurality of inductors (fig. 2, refs. LR3-LR5) and a plurality of PIN diodes (fig. 2, refs. D3-D5; col. 5, lines 50-55), each of the plurality of inductors having a first end and a second end (fig. 2), each of the plurality of inductors connected in parallel with a respective one of the plurality of pin does at the first end (fig. 2) and a common control node (fig. 2, CONT2) at the second end.

Regarding claim 22, Atokawa-'566 in view of Shimo, and in further view of Osofsky disclose the limitations of claim 14 as applied above. Further, Atokawa-'566 in view of Shimo, and in further view of Osofsky disclose the remaining limitations of the claim as applied to claim 21 above.

7. Claims 2, 3, 5, 6, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogel et al (US 6804262; hereafter "Vogel" – previously cited) in view of Atokawa, in further view of Shimo, and in further view of Osofsky.

Regarding claim 2, Vogel discloses upstream processing circuitry (fig. 3, refs. 114, 120, and 106) and downstream processing circuitry (fig. 3, refs. 108, 112, 116, and 114) coupled to a diplexer (fig. 3, ref. 104). Vogel does not disclose that the diplexer is having a high-pass filter, a low-pass filter, and a notch filter selectively coupled to the low-pass filter in response to indicium of a desired spectral region. However, Atokawa teaches the limitations Vogel does not explicitly disclose as applied to claim 1 above.

Atokawa teaches that, with the proposed variable bandwidth diplexer circuit, two passing bands are available for transmitting and receiving (col. 2, lines 22-30). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize the diplexer circuit as taught by Atokawa in the communications device of Vogel because two pass bands of transmission and two pass bands of reception could be accommodated. Further, Shimo and Osofsky teach the digitally operable switch connected in signal communication with the low-pass filter and responsive to signals from a microprocessor as applied in the rejection of claim 1 as being unpatentable over Atokawa in view of Shimo, and in further view of Osofsky, above.

Regarding claim 3, Vogel in view of Atokawa, in further view of Shimo, and in further view of Osofsky disclose the limitations of claim 2 as applied above. Further, Vogel discloses that the downstream processing circuitry comprises: a tuner (fig. 3, refs. 108); a demodulator (fig. 3, ref. 114; col. 10, lines 17-25); a first SAW filter (fig. 3, ref. 112; col. 9, lines 48-51) selectively coupled between said tuner and said demodulator; and a second SAW filter (fig. 3, ref. 116) selectively coupled between said tuner and said demodulator (col. 9, lines 55-60). Vogel does not explicitly disclose that the second filter is of a SAW filter type, but it is implied that the second filter (116) is functionally equivalent to the first filter (112) because they are used for the same purpose and in the same manner.

Regarding claim 5, Vogel in view of Atokawa, in further view of Shimo, and in further view of Osofsky disclose the limitations of claim 3 as applied above. Further,

Vogel discloses at least one selector (fig. 3, ref. 110) for selectively coupling the first SAW filter and the second SAW filter between the tuner and the demodulator.

Regarding claim 6, Vogel in view of Atokawa, in further view of Shimo, and in further view of Osofsky disclose the limitations of claim 3 as applied above. Further, in the communications device of Vogel in view of Atokawa, the tuner begins the downstream channel of the receiver

Regarding claim 12, Vogel in view of Atokawa, in further view of Shimo, and in further view of Osofsky disclose the limitations of claim 2 as applied above. Further, the device of Vogel in view of Atokawa is a cable modem as disclosed by Vogel (col. 2, lines 12-20).

8. Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogel in view of Atokawa-'566.

Regarding claim 2, Vogel in view of Atokawa-'566, in further view of Shimo, and in further view of Osofsky disclose upstream processing circuitry (fig. 3, refs. 114, 120, and 106) and downstream processing circuitry (fig. 3, refs. 108, 112, 116, and 114) coupled to a diplexer (fig. 3, ref. 104). Vogel does not disclose that the diplexer is having a high-pass filter, a low-pass filter, and a notch filter selectively coupled to the low-pass filter in response to indicium of a desired spectral region. However, Atokawa-'566 teaches the limitations Vogel does not explicitly disclose as applied above. Atokawa-'566 teaches that, with the proposed variable bandwidth diplexer circuit, two passing bands are available for transmitting and receiving (col. 2, lines 30-43) and overall miniaturization can be implemented (col. 2, lines 43-45). Therefore, it would

have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize the diplexer circuit as taught by Atokawa-'566 in the communications device of Vogel because two pass bands of transmission and two pass bands of reception could be accommodated using a small amount of circuitry. Further, Shimo and Osofsky teach the digitally operable switch connected in signal communication with the low-pass filter and responsive to signals from a microprocessor as applied in the rejection of claim 1 as being unpatentable over Atokawa in view of Shimo, and in further view of Osofsky, above.

Regarding claim 6, Vogel in view of Atokawa-'566, in further view of Shimo, and in further view of Osofsky disclose the limitations of claim 3 as applied above. Further, in the device of Vogel in view of Atokawa-'566, in further view of Shimo, and in further view of Osofsky, the high pass filter of Atokawa-'566 (fig. 1, "RECEIVING FILTER"; fig. 2, between "ANT" and "RX") would be connected to the tuner of Vogel because the high pass filter of Atokawa-'566 is the reception filter and should be connected to the reception tuner of Vogel.

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vogel in view of Atokawa-'566, in further view of Shimo, in further view of Osofsky, and in further view of Wilson et al (US 2002/0159511; hereafter "Wilson" – previously cited).

Regarding claim 9, Vogel in view of Atokawa-'566, in further view of Shimo, and in further view of Osofsky disclose the limitations of claim 1 as applied above. In the device of Vogel in view of Atokawa-'566, in further view of Shimo, and in further view of Osofsky, the frequency bands of the low pass filter and the low pass filter coupled to the

notch filter are not explicitly disclosed. However, Vogel does disclose that the low pass filter should have an operable range of 5 to 42 Mhz depending on the operation of the device (col. 7, lines 20-25) but is not limited to such an operating range. One skilled in the art would find it obvious that the operating range of a variable frequency low pass filter should accommodate all possible frequency ranges which may be desirable. In the DOCSIS device of Vogel in view of Atokawa-'566, at least two frequency ranges for the low pass filter are available. Vogel in view of Atokawa-'566, in further view of Shimo, and in further view of Osofsky does not disclose expressly passing signals less that 65Mhz as a possible selectable pass-band frequency range. However, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to utilize any other frequency range applicable to the device (i.e. 65Mhz). Applicant has not disclosed that the use of a 65Mhz low pass filter pass-band range provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with a 65Mhz low pass filter pass-band range as taught by Wilson (para. 0046) because it is readily utilized in a data over cable system as taught by Wilson (para. 0012). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a 65Mhz low pass filter pass-band as taught by Wilson in the device of Vogel in view of Atokawa-'566 because it is readily applicable to data over cable systems.

10. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogel in view of Atokawa, in further view of Shimo, in further view of Osofsky, and in further view of Miner et al (US 6690655; hereafter "Miner" – previously cited).

Regarding claim 4, Vogel in view of Atokawa, in further view of Shimo, and in further view of Osofsky disclose the limitations of claim 3 as applied above. Further, Vogel discloses that the bandwidth of the first SAW filter is 6Mhz (col. 9, lines 49-50). Vogel in view of Atokawa, in further view of Shimo, and in further view of Osofsky do not explicitly disclose that the second filter has a bandwidth of 8Mhz but discloses that the second filter changes the bandwidth of the first filter such that a second frequency selection system is defined (col. 9, lines 55-68). Vogel also discloses that various modifications of the frequency selection system may be made and suggests that the second filter and the first filter may be connected in parallel rather than in series (col. 10, lines 1-9). Additionally, Miner teaches that the fundamental difference in the Data-Over-Cable System Interface Specification (DOCSIS) system which is specified by Vogel (col. 2, lines 12-20) between domestic and international versions is the downstream channel bandwidth which is 6Mhz in the United States and 8Mhz internationally (col. 6, lines 10-11). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize the domestic and international bandwidth spectra (6Mhz and 8 Mhz, respectively) as taught by Miner for the frequency selection system of Vogel in view of Atokawa, in further view of Shimo, and in further view of Osofsky because the multi-mode bi-directional communications device could thereby the used both in the United States and abroad.

Regarding claim 13, Vogel in view of Atokawa, in further view of Shimo, in further view of Osofsky, and in further view of Miner disclose the limitations of claim 4 as applied above. Further, the device of Vogel in view of Atokawa, in further view of Shimo, in further view of Osofsky disclose, and in further view of Miner supports the domestic (North American) DOCSIS as well as international (European) DOCSIS as applied to claim 4 above. ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER

Jason M. Perilla
April 27, 2005

jmp